Attorney Docket No.: 001207.P006D Patent

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of:)
)
Ting et al.)
)
Serial No.: Not Yet Assigned)
)
Filed: December 5, 2001)
)
For: FLOOR PLAN FOR SCALABLE)
MULTIPLE LEVEL TAB)
ORIENTED INTERCONNECT)
ARCHITECTURE)
)

Art Unit: Not Yet Assigned

Examiner: Not Yet Assigned

"Express Mail" mailing label number: EL371002637US
Date of Deposit: 12/5/01
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D.C. 20231
Jenny Vicente
(Type or printed name of person mailing paper or fee)
Jenny Vicente
(Signature of person mailing paper or fee)
12/5/01

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

Sir:

Please enter the following preliminary amendment for the present patent application.

IN THE SPECIFICATION:

At page 2, please insert the following after the title:

--RELATED APPLICATIONS

The present patent application is a divisional of prior application no. 09/089,298, filed June 1, 1998, which is a continuation of prior application no. 08/434,980, filed May 4, 1995 both entitled FLOOR PLAN FOR SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE.--

IN THE CLAIMS

Please cancel claims 1-2 and add claims 3-34.

3. (New) A physical layout of a programmable logic circuit wherein the first programmable logic circuit comprises:

a first plurality of configurable cells including at least one Flip Flop cell configured to perform logic functions on logic signals, the configurable cells located along a first dimension;

a first set of routing lines selectively coupled to input/output ports of the configurable cells of the first plurality of configurable cells through a first set of switches; and

the first set of switches comprising a first memory and passgate array, the first memory and passgate array and the first plurality of configurable cells located adjacent to each other along a second dimension and a portion of at least one routing line of the first set of routing lines located inside the first memory and passgate array along the first dimension.

4. (New) The physical layout of the programmable logic circuit of Claim 3, further comprising a second set of switches selectively coupled to the first set of routing lines to extend the first set of routing lines along the first dimension, a portion of the second set of switches comprising a second memory and passgate array, the second memory and passgate array and the first memory and passgate array located adjacent to each other along the first dimension.

5. (New) The physical layout of the programmable logic circuit of claim 4, further comprising a third set of switches extending the first set of routing lines along the second dimension, the third set of switches comprising a portion of a third memory and passgate array, the third memory and passgate array and the first memory and passgate array located adjacent to each other along the second dimension.

6. (New) The physical layout of the programmable logic circuit of claim 4, further comprising:

a second plurality of configurable cells and a second set of routing lines, the configurable cells of the second plurality of configurable cells located along the first dimension;

the second set of routing lines selectively coupled to input/output ports of the configurable cells of the second plurality of configurable cells through a fourth set of switches;

the fourth set of switches comprising a fourth memory and passgate array, the fourth memory and passgate array and the second plurality of configurable cells located adjacent to each other along the second dimension; and

the fourth memory and passgate array and the second memory and passgate array located adjacent to each other along the first dimension.

7. (New) The physical layout of the programmable logic circuit of claim 6, wherein the second set of switches selectively couples the first set of routing lines to the second set of routing lines along the first dimension.

8. (New) The physical layout of the programmable logic circuit of claim 5, further comprising:

a third plurality of configurable cells and a third set of routing lines, the configurable cells of the third plurality of configurable cells located along the first dimension;

the third set of routing lines selectively coupled to input/output ports of the configurable cells of the third plurality of configurable cells through a fifth set of switches;

the fifth set of switches comprising a fifth memory and passgate array, the fifth memory and passgate array and the third plurality of configurable cells located adjacent to each other along the second dimension; and

the fifth memory and passgate array and the third memory and passgate array located adjacent to each other along the second dimension.

9. (New) The physical layout of the programmable logic circuit of claim 8, wherein the second set of switches selectively couples the first set of routing lines to the third set of routing lines along the second dimension.

10. (New) The physical layout of the programmable logic circuit of claim 8, further comprising a fourth set of routing lines selectively coupled to the input/output ports of the configurable cells of the first and second plurality of configurable cells through a sixth set

of switches, the sixth set of switches comprising a portion of the third memory and passgate array.

11. (New) The physical layout of the programmable logic circuit of claim 10, wherein the fourth set of routing lines are selectively coupled to the input/output ports of the configurable cells of the third plurality of configurable cells through the fifth set of switches.

12. (New) The physical layout of the programmable logic circuit of claim 6, further comprising:

a fourth plurality of configurable cells and a fifth set of routing lines, the configurable cells of the fourth plurality of configurable cells located along the first dimension;

the fifth set of routing lines selectively coupled to input/output ports of the configurable cells of the fourth plurality of configurable cells through a seventh set of switches;

the seventh set of switches comprising a sixth memory and passgate array, the sixth memory and passgate array and the fourth plurality of configurable cells located adjacent to each other along the second dimension; and

the sixth memory and passgate array and the third memory and passgate array located adjacent to each other along the second dimension.

13. (New) A physical layout of a programmable logic circuit wherein the programmable logic circuit comprises:

a first plurality of configurable cells and a second plurality of configurable cells configured to perform logic functions on logic signals;

a first set of routing lines selectively coupled to a plurality of input ports and at least one output port of each configurable cell of the first and second plurality of configurable cells through a first set of switches;

the first set of switches comprising a first memory and passgate array located between the first and second plurality of configurable cells along a first dimension, and a portion of at least one routing line of the first set of routing lines located inside the first memory and passgate array along a second dimension.

14. (New) The physical layout of the programmable logic circuit of Claim 13, further comprising a second set of switches to selectively couple the first set of routing lines to at least one routing line of a second set of routing lines, a portion of the second set of switches comprising a first driver logic and a second memory and passgate array, and

the first driver logic, the second memory and passgate array, and the second plurality of configurable cells are located adjacent to each other along the first dimension.

15. (New) The physical layout of the programmable logic circuit of Claim 14, wherein the second set of switches comprises components selected from the group consisting of the switches, the programmable passgates and the program controlled drivers/receivers.

16. (New) The physical layout of the programmable logic circuit of Claim 14, wherein the first driver logic and the second memory and passgate array further comprise a driver logic array and a memory and passgate array located adjacent to each other along the first dimension.

17. (New) The physical layout of the programmable logic circuit of Claim 14, wherein the second set of switches further comprise a second driver logic and a third memory and passgate array, and

the second driver logic, the third memory and passgate array and the first memory and passgate array are located adjacent to each other along the second dimension.

18. (New) The physical layout of the programmable logic circuit of Claim 17, wherein the second driver logic, the third memory and passgate array and the first plurality of configurable cells are located adjacent to each other along the second dimension.

19. (New) The physical layout of the programmable logic circuit of Claim 17, wherein the second driver logic, the third memory and passgate array and the second plurality of configurable cells are located adjacent to each other along the second dimension.

20. (New) The physical layout of the programmable logic circuit of Claim 17, wherein the second driver logic and the third memory and passgate array further comprise a driver logic array and a memory and passgate array located adjacent to each other along the second dimension.

21. (New) The physical layout of the programmable logic circuit of claim 17, further comprising a third set of switches to selectively couple a first portion of routing lines of the second set of routing lines located in the first dimension to a second portion of routing lines of the second set of routing lines located in the second dimension,

the third set of switches comprise a turn network, and the turn network, the first driver logic and the second memory and passgate array are located adjacent to each other along the second dimension, and

the turn network, the second driver logic and the third memory and passgate array are located adjacent to each other along the first dimension.

22. (New) The physical layout of the programmable logic circuit of claim 13, further comprising a third set of routing lines selectively coupled to the input/output ports of the configurable cells of the first plurality of configurable cells, a portion of the third set of routing lines located between the first plurality of configurable cells and the first memory and passgate array along the first dimension.

23. (New) The physical layout of the programmable logic circuit of claim 13, further comprising a fourth set of routing lines selectively coupled to the input/output ports of the

configurable cells of the second plurality of configurable cells, a portion of the fourth set of routing lines located between the second plurality of configurable cells and the first memory and passgate array along the first dimension.

24. (New) A method for generating a physical layout of a programmable logic circuit comprising:

providing a first plurality of configurable cells configured to perform logic functions on logic signals, the configurable cells located along a first dimension;

selectively coupling a first set of routing lines to input/output ports of the configurable cells of the first plurality of configurable cells through a first set of switches, wherein the first set of switches comprises a memory and passgate array;

locating the first memory and passgate array adjacent to the first plurality of configurable cells along a second dimension; and

locating a portion of at least one routine line of the first set of routing lines inside the first memory and passgate array along the first dimension.

25. (New) The method as set forth in claim 24, further comprising:

providing a third set of switches extending the first set of routing lines along the second dimension, the third set of switches comprising a portion a third memory and passgate array;

locating the third memory and passgate array adjacent to the first memory and passgate array along the second dimension.

26. (New) The method as set forth in claim 24, further comprising:

providing a second plurality of configurable cells and a second set of routing lines;

locating the second plurality of configurable cells along the first dimension;

selectively coupling the second set of routing lines to input/output ports of configurable cells of the second plurality of configurable cells through a fourth set of switches, wherein the fourth set of switches comprises a fourth memory and passgate array;

locating the fourth memory and passgate array and the second plurality of configurable cells adjacent to each other along the second dimension; and

locating the fourth memory and passgate array and the second memory and passgate array adjacent to each other along the first dimension.

27. (New) A method for generating a physical layout of a programmable logic circuit comprising:

providing a first plurality of configurable cells and second plurality of configurable cells configured to perform logic functions on logic signals;

selectively coupling a first set of routing lines to a plurality of input ports and at least one output port of each configurable cell of the first and second plurality of configurable cells through a first set of switches, the first set of switches comprising a first memory and passgate array;

locating the first memory and passgate array between the first and second plurality of configurable cells along a first dimension; and

locating a portion of at least one routing line of the first set of routing lines inside the first memory and passgate array along a second dimension.

28. (New) The method as set forth in claim 27, further comprising:

selectively coupling through a second set of switches the first set of routing lines to at least one routing line of a second set of routing lines, a portion of the second set of switches comprising a first driver logic and a second memory and passgate array;

locating the first driver logic, the second memory and passgate array and the second plurality of configurable cells adjacent to each other along the first dimension.

29. (New) The method as set forth in claim 28, wherein the second set of switches further comprise a second driver logic and a third memory and passgate array, the method further comprising locating the second driver logic, the third memory and passgate array and the first memory and passgate array adjacent to each other along the second dimension.

30. (New) The method as set forth in claim 29, further comprising locating the second driver logic, the third memory and passgate array and the first plurality of configurable cells adjacent to each other along the second dimension.

31. (New) The method as set forth in claim 29, wherein the second driver logic and the third memory and passgate array further comprises a driver logic array and a memory and passgate array located adjacent to each other along the second dimension.

32. (New) The method as set forth in claim 29, further comprising:

selectively coupling, through a third set of switches comprising a turn network, a first portion of routing lines of the second set of routing lines located in the first dimension to a second portion of routing lines of the second set of routing lines located in the second dimension;

locating the turn network, the first driver logic and the second memory and passgate array adjacent to each other along the second dimension; and

locating the turn network, the second driver logic and the third memory and passgate array adjacent to each other along the first dimension.

33. (New) The method as set forth in claim 27, further comprising:

selectively coupling a third set of routing lines to input/output ports of the configurable cells of the first plurality of configurable cells;

locating a portion of the third set of routing lines between the first plurality of configurable cells and the memory and passgate array along the first dimension.

34. (New) The method as set forth in claim 27, further comprising:

selectively coupling a fourth set of routing lines to input/output ports of the configurable cells of the second plurality of configurable cells; and

locating a portion of the fourth set of routing lines between the second plurality of configurable cells and the first memory and passgate array along the first dimension.

REMARKS

Claims 3-34 correspond with claims 25-56 that were subject to a restriction requirement in the parent case serial no. 09/089,298, filed June 1, 1998.

Applicants respectfully submit that the claims are in condition for allowance.

Please charge any shortages and credit any overcharges to our Deposit Account No. 02-2666.

Respectfully submitted,

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

Dated: DEC 5, 2001

Sheryl Sue Holloway
Reg. No. 37,850

12400 Wilshire Blvd.
Seventh Floor
Los Angeles, CA 90025-1026
(408) 720-8300

VERSON TO SHOW CHANGES MADE

IN THE SPECIFICATION:

At page 2, please insert the following after the title:

RELATED APPLICATIONS

The present patent application is a divisional of prior application no. 09/089,298, filed June 1, 1998, which is a continuation of prior application no. 08/434,980, filed May 4, 1995 both entitled FLOOR PLAN FOR SCALABLE MULTIPLE LEVEL TAB ORIENTED INTERCONNECT ARCHITECTURE.